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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,940	03/17/2006	Desmond Bryan Mills	3003-1169	1500
465 7590 02/13/2009 YOUNG & THOMPSON 209 Madison Street Suite 500 ALEXANDRIA, VA 22314			EXAMINER STOKLOS, JOSEPH A	
			ART UNIT 3762	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/559,940

Applicant(s)

MILLS ET AL.

Examiner

JOSEPH STOKLOSA

Art Unit

3762

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 33-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 33-63 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/CDC)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 33-35 and 37-60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Newly added claim limitations "self-test means is limited to generation of self-testing signals and...", in combination with the other claimed elements, lacks specification support within the original disclosure.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 33-35, 37-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claim 33 recites the limitation that the self test be "activated independently of operation of the medical device and not by a signal from a processor associated with said medical device." Examiner considers this limitation to be vague and indefinite, as the term associated renders the claim vague. Applicant claims the self test components generate a self test independent from any processor associated with the medical

device; however examiner considers this to be contradictory, for each component must have some independent circuitry or logic, which Examiner considers to be a processor, that will initiate an activation signal to initiate the self test, and each independent circuitry or logic is therefore inherently associated with the medical device. For the purpose of examination Examiner will consider the limitation to only require that the activation signal be generated from a processor/circuitry/logic that does not control the function of the device, but rather is only limited to generation of self testing signals. The claims should be amended accordingly.

Claim Rejections - 35 USC § 102/103

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 33-41, 43, 47, 51, 53-54, and 58-63 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ochs et al. (US 5,899,925).

10. Ochs discloses a self testing system with a plurality of components that carry out self test routines on the various components (e.g. Col. 3, lines 60-Col. 4, line 9). Ochs discloses the system monitor to generate the testing activation signal for the various components (e.g. Col. 3, line 47-59). Ochs discloses the results may be then passed to a common processor, CPU (element 16; Col. 3, line 56-60). Examiner considers this disclosure to satisfy the claimed limitations in that Ochs discloses the system monitor for generating the activation signal for the self tests and not the AED CPU, element 16, which is associated with the medical device and further in light of the fact that Ochs discloses the system monitor to be powered independently of the AED (Col. 4, line 14-19). Further Ochs discloses that system monitor is a controller and not a processor as seen in Fig. 2.

11. In the alternative, Ochs further discloses the benefit to having the system monitor generate the self test signals and not the CPU. Ochs discloses that the system monitor would free up the load on the CPU and allow the CPU to focus on other tasks such as operating the device. If one considers the system monitor to be a processor associated

with the medical device and in light of Ochs explicit teaching of the benefits to not using a central processor for generating self test, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by Ochs with having individual system monitors to generate test signals for the various components since such a modification would provide the predictable results of minimizing the load on one processor which could produce a delay in operation of the device.

12. With regard to claim 35 and 36, Examiner considers the system gate array and memory to constitute a summator which receives test results and performs basic discrete logic functions before passing the results to the CPU (e.g. Col. 3, line 30-45). In the alternative Examiner considers the self test system to inherently possess a summator, in that an indication of whether the self test passed or failed is necessary to be indicated on the LCD display. Ochs also discloses indicators in the form of displays and audio alerts.

13. With regard to claims 39 and 40, Ochs discloses each component for having a communication means for transmitting the self test data to the gate array and then on to the CPU. It is Examiners position that with each component having a communication channel that, this is a single and separate data link.

14. With regard to claim 41, Ochs discloses the system gate array may be a microcontroller in the form of an integrated circuit (Col. 3, line 33-34).

15. With respect to claim 42, Ochs discloses the system gate array to feed into the CPU as seen in Fig. 2, therefore the functional connection between the gate array and the CPU renders the gate array to be part of the main CPU.

16. With regard to claim 47, Ochs discloses a self test being triggered by the completion of a test by another component (Col. 5, lines 53-56, and Col. 4, lines 29-31). Where a self test is performed on the ambient condition sensor which triggers testing of the voltage impedance.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 42, 44-46, 48-50, 52, and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochs as applied above.

19. With regard to claims 42, 48-50, and 57 Ochs discloses the invention as claimed but fails to teach the summator including a subtractor, a digital signal processor with a base station activation when the device is placed within the base station, and testing the power source prior to other components. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by Ochs with the use of a subtractor, a digital signal processor with a base station activation when the device is placed within the base station, and checking the power source prior to the other components, since such modifications would provide the

predictable results of a subtractor for performing the basic discrete logic functions taught by Ochs, and the digital signal processor within a base station to provide the predictable results of accurate, reliable and precise signal data for optimum therapy administration and a signal from a server or base station and reliable and safe device manipulation from a remote location and checking the power source prior to other components provides the predictable results of letting the system know if the it has enough power to even perform the other system component tests and the performing of other component tests may be moot if the system does not have a valid power source which will be able to perform the defibrillation in the first place.

20. With regards to claims 44-46, 52, and 55-56 Ochs disclose the essential features of the claimed invention except for transmitting data in the form of pulses with a whole number in the form of x^2 , a number of pulses = 1024 pulses, and a first voltage of between 450V or a second voltage of 40V. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include transmitting data in the form of pulses with a whole number in the form of x^2 a number of pulses = 1024 pulses and a first voltage of between 450V or a second voltage of 40V, since such modifications would provide the predictable results of providing a known method of transmitting data effectively in the digital signal processing field with known integers that are compatible with the bit processing systems, and the voltage being within 450V or 40V to ensure a sufficient voltage is able to be generated to perform defibrillation therapy later required to save a patient's life.

21. Moreover, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272,205 USPQ 215 (CCPA 1980). (See MPEP 2144.05).

Response to Arguments

22. Applicant's arguments filed 12/11/2008 have been fully considered but they are not persuasive.

23. Applicant argues that the self-test means is generated from the system monitor, 12. Examiner acknowledges that the self-test means is generated from the system monitor; however, Examiner does not consider the system monitor to be a processor associated with the operation of the medical device. Ochs explicitly teaches that the CPU does not oversee the generation and control of self-testing the individual components for the sake of allowing the CPU to focus on other tasks (e.g. Col. 4, line 12-13). In light of this, it is clear that the system monitor oversees the self-testing and the CPU is not involved in the self-testing control and rather is only the common processor associated with the device. Further, Examiner is of the position that if one considers the system monitor to be a processor, it would have been obvious to use individual self-test generating means as explained above in paragraph 11.

24. Applicant argues that Ochs fails to teach an activation signal for the ECG testing. Examiner reminds applicant that this is not a ***claimed*** limitation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH STOKLOSA whose telephone number is (571)272-1213. The examiner can normally be reached on Monday-Friday 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Angela Sykes can be reached on 571-272-4955. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/5/2009